PVP 14

Code: EE5T6

III B.Tech - I Semester – Regular Examinations - December 2016

LINEAR AND DIGITAL INTEGRATED CIRCUIT APPLICATIONS

(ELECTRICAL & ELECTRONICS ENGINEERING)

Duration: 3 hours Max. Marks: 70

PART – A

Answer ***all*** the questions. All questions carry equal marks

11 x 2 = 22 M

1.

a) Explain why the open-loop op-amp configurations are not used in linear applications?

b) What is the output voltage and approximate output current of an op-amp when the load resistor of an op-amp is short circuited?

c) Justify the statement that op-amp is a Voltage Controlled Voltage source.

d) List the advantages and disadvantages of Switched Capacitor filter.

e) What is frequency stability in oscillator and give its significance?

f) List the features of 555 timer.

g) List the basic building blocks of the discrete Phased Locked Loop.

h) Draw the logic diagram of 74x138 3-to-8 decoder.

i) Write a design procedure of combinational circuits.

j) List the applications of Flip-flops.

k) Write the specifications of shift register IC's.

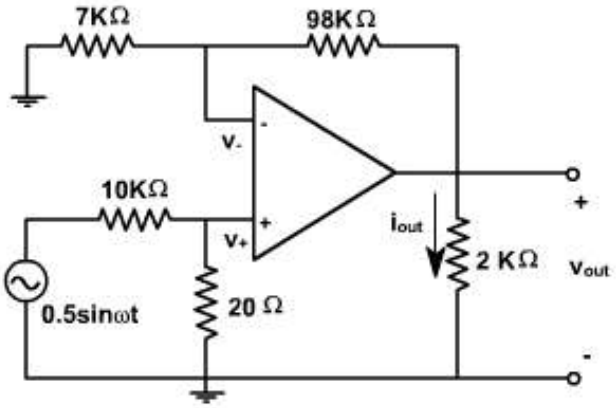
PART – B

Answer any *THREE* questions. All questions carry equal marks. 3 x 16 = 48 M

2. a) Define the following op-amp parameters 8 M

*i)*Differential input resistance *ii)* input offset voltage *iii)*offset voltage adjustment range *iv)* Slew rate

b) Find V_{out} & I_{out} for the circuit shown below. 8 M



3. a) Explain the operation of RC phase shift oscillator with neat sketch. 8 M

b) Assuming suitable data design for a first order low pass filter at cut-off frequency of 1KHz with a pass band gain of 2. 8 M

4. a) Design a Monostable Multivibrator using 555 timer to produce a pulse width of 100 msec. 8 M

b) Give the functional block diagram of VCO NE566 and explain its working and derive the necessary expression for free running frequency. 8 M

5. a) Design a 4 to 16 decoder using two 74x138 decoders. 8 M

b) Design a parallel binary adder. 8 M

6. a) Draw the logic diagram of 74x194 shift register and explain the operation. 8 M

b) Design a circuit to convert a T-flipflop to J-K flipflop. 8 M